Amendments to the Specification:

Kindly replace paragraph [0002] with the following amended paragraph:

[0002] A problem in the art has been discovered to exist in connection with an excessive field oxide recess for thin silicon SOI. The excessive field oxide recess leads to ~~MOAT~~ moat formations or voids occurring around bitcells and other structures in SOI. The ~~MOATs~~ moats have been found to form as a result of HF penetration that etches an insulative fill material, such as HDP, from the sidewalls of Si (at an interface between the Si and trench isolation material), coupled with areas of weak oxide at the top of a BOX (bottom oxide), and at the top Si interface. Etching of the two weak oxide regions accelerates the removal of the isolation material from around a given structure, thereby causing recession to occur into the BOX, thus undesirably forming a ~~MOAT~~ moat or void.

Kindly replace paragraph [0003] with the following amended paragraph:

[0003] In one example, a problem exists in the area of weak oxide found at the top of the BOX layer near the interface of a ~~200A thick~~ 200Å thick liner. This area of weak oxide functions as a stress relief mechanism. When the stress relief mechanism is coupled with the recession of HDP at the sidewalls of the shallow trench isolation (STI) corner region, formation of ~~MOATS~~ moats occurs, leading to formation of poly stringers and depressed device yields.

Kindly replace paragraph [0012] with the following amended paragraph:

[0012] According to the present disclosure, the embodiments eliminate various mechanisms in the formation of ~~MOAT~~ moat defects. For example, the embodiments eliminate a first mechanism that starts the formation of ~~MOAT~~ moat defects. Secondly, the embodiments address a second area that enables the ~~MOAT~~ moat defect, corresponding to the weak oxide at the bottom of the liner/top BOX and bottom Si interface. Accordingly, by eliminating the first and second mechanisms, the recession of the HDP by one or more HF cleans does not lead to any voids or areas for POLY stringers. Moreover, leakage current is diminished and yields for devices are improved. In one embodiment, the problems in the art are overcome by a re-

engineering of an SOI integration for Thin SOI. Such a method includes, for example, changes in thicknesses for a PAD-Ox, a liner oxide, and an HDP fill process.

Kindly replace paragraph [0013] with the following amended paragraph:

[0013] The first mechanism of the ~~MOAT~~ moat defect was discovered at the interface of the oxide and nitride, which corresponded to an approximate 35Å undercut. The undercut was created by a pre-clean 35 Å HF that was used prior to the trench liner deposition. The Oxide thickness was on the order of 145 Å. The second mechanism was the area under the 200A liner at the top of the box/top of the bottom Si interface. There was significant overlap of the liner that prohibited a uniform fill at the bottom of the liner. Accordingly, the area included a void at the bottom, which became a stress relief point. Through subsequent processing, the void at the top is recessed below the Si, due to HF etching and merges with the void at the bottom, thus developing into a ~~MOAT~~ moat defect that extends into the BOX.

Kindly replace paragraph [0036] with the following amended paragraph:

[0036] Referring now to Figure 18, the two views indicated by reference numerals 122 and 124 are similar to those shown in Figure 17, wherein the SOI semiconductor device 110 has been further processed with a subsequent gate patterning step where defined on an STI active region (view 124 of Figure 10), and where not-defined, the polysilicon and gate oxide are removed (view 122 of Figure 10). Accordingly, views 122 and 124 of Figure 18 have the following differences. In view 122 of Figure 18, polysilicon 150 and gate oxide 148 are removed, and no polysilicon remains that would cause a short as in the prior integration of Figures 1-9. In view 124 of Figure 18, the gate polysilicon is free of any active regions with moats as in the prior integration of Figures 1-9. Accordingly, hard bit failures are advantageously avoided in an array of the SOI semiconductor ~~device 10~~ device 110.